ABSTRACT OF THE DISCLOSURE

A system is disclosed that detects data forwarding clock errors including both missing and additional clock signals. The system provides for a phase locked loop (PLL) that locks onto a data forwarding source synchronous clock signal wherein the PLL outputs a system clock whose frequency is the average of the data forwarding clock frequency. The data forwarding clock signals and the system clock signals are counted separately and when a discrepancy occurs the receiving system is informed that an error has occurred. The receiving system will handle the error in its routine fashion. The counters and the PLL are synchronized to be sure that the PLL has acquired a lock before the error detection is enabled.